UNSIGNED HARDCOPY
NOT CONTROLLED

SUBJECT:	Printed Wire Board Fabrication
APPROVED BY	Manager, Hardware Engineering
STATUS	Maintenance Revision
PURPOSE	Extension to the master drawing for the fabrication and inspection of rigid single, double-sided, and multilayer printed wiring boards. Provides guidance to its users in a conformable manner for the manufacture of printed wiring boards. In the event of a conflict between the text of this instruction and the references cited herein, the text of this instruction shall take precedence.
AFFECTED FUNCTIONS	Hardware Engineering Manufacturing

REFERENCES		
	ASTM-E53	Standard Method for Chemical Analysis of Copper
	EIA-IS-5A	Packaging Material Standards for ESD Sensitive Items
	IPC-SM-840	Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards
	MIL-P-13949	Plastic Sheet, Laminate, Metal-Clad (for Printed Wiring Boards)
	J-STD-004	Requirements for Soldering Fluxes
	MIL-C-14550	Copper Plating (Electrodeposited) (canceled-replaced by AMS 2418 Plated Copper for certain applications)
	MIL-D-3464	Desiccants, Activated, Bagged, Packaging Use and Static Dehumidification
	MIL-I-8835	Indicator, Humidity, Card, Chemically Impregnated
	MIL-G-45204	Gold Plating, Electrodeposited
	MIL-P-55110	General Specifications for Printed Wiring Boards
	SAE-AMS-P-81728	Plating, Tin-Lead (Electrodeposited)
	MIL-STD-2000	Standard Requirements for Soldering Electrical and Electronic Assemblies (canceled- no replacement)
	J-STD-006	Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

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DEFINITIONS

Annular ring**.** That portion of conductive material completely surrounding a hole.

Dewetting. A condition which results when the molten solder coats a surface and then recedes to leave irregularly shaped mounds of solder that are separated by areas covered with a thin film of solder and with the basis metal not exposed.

Fusing. The combining of metals by means of melting, blending, and solidification.

Lands. A portion of a conductive pattern that is usually used for making electrical connections for component attachment, or both.

Master drawing. A document that shows the dimensional limits or grid locations that are applicable to any and all parts of a product to be fabricated, including the arrangement of conductors and nonconductive patterns or elements; the size, type, and location of holes; and any other necessary information.

Nonwetting. The partial adherence of molten solder to a surface that it has contacted and basis metal remains exposed.

Plated–through hole. A hole with plating on its walls that makes an electrical connection between conductive patterns on internal layers, external layers, or both of a printed board.

Solder mask. A resist that provides protection from the action of solder.

Solderability. The ability of a metal to be wetted by molten solder.

Test Specimen. A portion of the printed circuit board not greater than 2 inches x 2 inches (5.08 cm x 5.08 cm) containing as much of a representative sampling of all hole sizes and other circuitry, or the complete board if it is smaller than this size.

Via hole. A plated–through hole that is used as an interlayer connection in which there is no intention to insert a component lead or other reinforcing material.

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Warp (bow). The deviation from flatness of a board characterized by a roughly cylindrical or spherical curvature, such that if the board is rectangular, its four corners are in the same plane.

Wetting. The formation of a relatively uniform, smooth, unbroken, and adherent film of solder to a basis metal.

INSTRUCTION

1. Requirements

1.1 Printed wiring delivered under this instruction shall meet the qualifications and performance requirements of MIL-P-55110 and the requirements of the approved master drawing. In addition, all printed–wiring boards shall meet the requirements as specified herein.

1.2 Material.

a. *S*ingle-and double-sided boards. The base material for laminates shall be in accordance with MIL-P-13949, type GFN.

b. Multilayer boards. The base material for laminates shall be in accordance with MIL-P-13949, type GFN. Resin material for preimpregnated material shall be in accordance with MIL-P-13949, type GF.

1.3 Plating**.** All exposed conductive patterns (plated–through holes, terminal areas, etc.) shall be tin-lead plated or solder coated. When other platings are used on the same printed wiring board in conjunction with tin-lead plating, the area of overlap shall be kept to a minimum, and no exposed copper shall be permitted at the interface between the other plating and the tin-lead plating. No solder shall be under other plating.

a. Electroless copper plating. An electroless deposition system shall be used as a preliminary process for providing the conductive layer over nonconductive materials for subsequent electrodeposition of metal in plated–through holes.

b. Electrolytic copper plating. All electrolytically deposited copper plating shall be performed in accordance with MIL-C-14550 and shall have a

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minimum purity of 99.5 percent as determined by ASTM–E53. The minimum thickness shall be .001 inch (0.03 mm).

c. Tin–lead plating. Tin-lead plating shall be in accordance with SAE-AMS-P-81728. Fusing shall be required on all tin-lead plated surfaces. The tin-lead shall be .0005 inch (0.013 mm) thick minimum (before fusing), as plated on the surface.

d. Refer to Paragraph 2.8 for solder-coated boards (i.e., hot-air, solder-leveled).

e. Unsupported holes. Tooling holes, mounting holes, holes without lands (pads), and holes with a pad diameter smaller than the hole diameter shall not be plated.

1.4 Board edge type connector contacts. When board edge type connectors are shown on the master drawing, they shall be plated with copper to a thickness equal to that of the remaining conductive pattern. The contacts shall be plated with gold over low–stress nickel. Gold shall be a minimum of .00005 (50 millionths) inch (0.001 mm) and a maximum of .0001 (100 millionths) inch (0.003 mm) thick, and shall be type 1, grade C, class 1 in accordance with MIL-G-45204. Low-stress nickel shall be a minimum of .0002 inch (0.005 mm) thick. Surface roughness of the plated contacts shall not exceed 60 microinches (0.002 mm). The leading edge of the contact shall be tapered and shall not extend to the edge of the board.

1.5 Identification marking. Individual printed–wiring boards and quality conformance test circuitry shall be identified on the master drawing.

a. The markings shall include the design activity's CAGE Code, part number, and Rev level and should be on the first line. The manufacturer's CAGE Code number and a four-digit date code shall be etched in copper or stamped with a nonconductive, permanent, fungistatic ink below or near the part number on the solder side of the board as follows:

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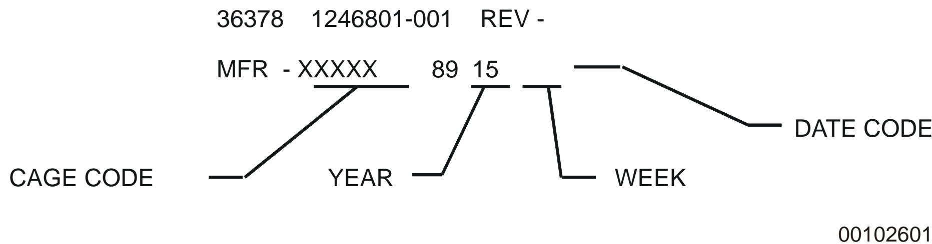

b. The identification markings shall be in accordance with the marking requirements of MIL-P-55110. Etched copper is preferred.

1.6 Solder mask. Solder masks utilizing Photocircuits PC401, PC501, alpha metal TM62, Maccumask 9446, or equivalent are acceptable. Hysol SR 1010 or SR 1000 are NOT acceptable. New or equivalent unapproved solder masks shall have prior L-3 Communications Corporation, Link Simulation & Training Division (hereafter referred to as Link) approval. Solder masks shall be applied to the front and rear layers of Type II and Type III boards. Type I boards require a solder mask only on the circuit side. The solder mask shall conform to IPC-SM-840, Class 3. Boards with pads-only construction do not require solder mask unless specified by design. Solder Mask Over Bare Copper (SMOBC) is acceptable construction.

1.7 Via holes. The actual hole size of via holes is not critical; however, size shall meet the dimensions specified on the master drawing for all new printed–wiring designs released after January 1989. For older printed-wiring boards released prior to January 1989, finished via hole diameter may vary between -.009 inch and +.003 inch (- 0.229 mm and +0.076 mm) of the specified diameter on the master drawing.

Via holes may be filled with solder.

1.8 Type 3 board testing. All Type 3 boards shall be electrically tested in accordance with MIL-P-55110. Sampling shall not be allowed.

All boards which have passed an electrical test shall be permanently marked indicating electrical test certification.

2. Quality Assurance Provisions

2.1 General. All boards are subject to the quality provisions as specified in this instruction and the following paragraphs.

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2.2 Coupons, microsections, and test data shall be retained by the supplier (reference MIL-P-55110, section 4.7) for a period of three years and made available to Link upon request. Additional microsections may be requested by Link for analysis of defects.

2.3 Solder mask. There shall be no evidence of solder mask or legend/reference designators in any hole or on the surface area of the minimum annular rings in accordance with MIL-P-55110.

2.4 Subcontractor quality requirements. Subcontractors providing boards to Link shall have a quality program which will assure the delivery to Link of only boards which meet the requirements of the purchase agreement and the master drawing.

2.5 One additional board for each different date code shall be supplied for solderability testing as specified in Paragraph 2.7.

2.6 Date code. Printed–wiring boards with a date code more than six months prior to the date of receipt shall be resolderability tested by Link prior to acceptance.

2.7 Solderability test. All printed-wiring boards shall be capable of passing the Wave Solder Test performed at Link and the Solder Float Test defined below.

a. General. The solderability determination is made to verify that the printed wiring fabrication processes and storage have had no adverse effect on the solderability of the printed-wiring boards. This is determined by evaluating the ability of those portions of the printed–wiring board normally soldered to be wetted by a new coat of solder. Determination is judged by nondestructive methods.

b. Material.

(1) Solder. The solder shall be compositions noted in J-STD-006. The solder composition shall be analyzed in accordance with MIL-STD-2000 (reference).

(2) Flux. The soldering flux shall be liquid, type R, conforming to j-std-004.

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(3) Flux remover. The flux remover shall be either isopropyl alcohol or another suitable solvent.

c. Equipment.

(1) Solder pot. A thermostatically controlled solder pot of adequate dimension to accommodate the specimen and containing no less than five pounds of solder shall be used. The solder shall be maintained at a temperature of 500 °F ± 10 °F (260 °C ± 5.5 °C).

(2) Shear. A tool utilized to cut the printed–wiring board to the test specimen size.

(3) Specimen handling tool. Stainless steel tongs or another specially designed tool of stainless steel shall be used to handle the specimen only by the edges.

(4) Optical equipment. An eye loupe or microscope with magnification up to 10X shall be used for inspection.

d. Procedure.

(1) Immerse the test specimen in flux and after removal drain it by standing on edge for 30 seconds.

(2) Skim the solder pot to remove dross.

(3) Slide the specimen onto the surface of the molten solder.

(4) Allow the specimen to float one second and then begin timing.

(5) Remove the specimen by sliding it from the surface after a maximum of five seconds. Heavy internal ground plane, multilayer and thick (.125 inch [3.175 mm]) boards may require more than five seconds for hole filling. If such a condition exists, hole–filling time should be agreed on between supplier and Link.

(6) Allow the solder to solidify while holding the specimen still and in a horizontal position above the solder surface.

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(7) Remove all flux with flux remover.

(8) This is a test method, and the solder float and wetting time shall not be construed as having a relationship with actual production soldering times.

e. Solderability evaluation.

(1) Surface conductor. Criteria for acceptable solderability calls for a minimum of 95 percent of the surface being tested to exhibit good wetting. The balance of the surface may contain only small pin holes, dewetted areas, and rough spots, provided such defects are not concentrated in one area. There shall be no nonwetting or exposed base metal within the evaluated area. An area of .125-inch (3.175-mm) width from each edge of the test specimen and areas contacted by the handling tool shall not be evaluated.

(2) Plated–through hole. The specimen is acceptable if solder has fully wetted the sides of the hole and over the knees onto the lands at the top and bottom of the board. (See Figure 1.)

(a) There shall be no nonwetting, exposed base metal, blow holes, or voids in and/or on any platedthrough hole.

(b) Plated–through holes less than .200 inch (5.08 mm) from the edges of the specimen shall not be evaluated.

(c) Partially filled holes are acceptable, provided they meet the criteria in paragraph 2.7e(2) and 2.7e(2)(a).

f. Inspection. Optical equipment specified in paragraph 2.7c(4) shall be used for the solderability evaluation.

Pretreatments. The occurrence of outgassing, which may result in blow holes, measling, blisters, or delamination, may be reduced by baking the printed–wiring board (test specimen) prior to testing. This pretreatment must be agreed on between supplier and Link before use.

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g. Solder–coated boards (i.e., hot-air, solder-leveled boards).

(1) Solder thickness shall be a minimum of .0003 inch (0.008 mm) at five (5) sample locations across the board surface. Measurement is to be done via microsectioning or x-ray florescence, and the data for the five sample locations made available to Link.

(2) Ionic contamination must be checked and a data printout supplied with each lot shipped.

3. Preparation For Delivery

3.1 Packaging. After fabrication completion, all printed–wiring boards shall be individually packaged in a self-sealing ("zipper lock") antistatic bag in accordance with EIA-IS-5A, Dow Chemical Chiploc DP, 3M 2110E, or Link-approved equivalent. Each bag shall contain a desiccant in accordance with MIL-D-3464 and humidity indicator in accordance with MIL-I-8835. The humidity indicator shall be visible for inspection without opening the package. At no time shall the boards be wrapped in paper or plastic containing sulfuric or hydrochloric residues which might outgas. The size of the bag shall be appropriate for the size of the board and allow easy insertion or removal of the board.

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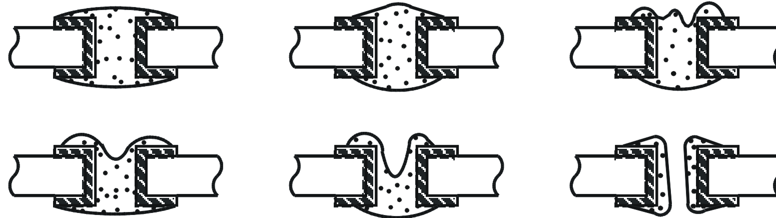
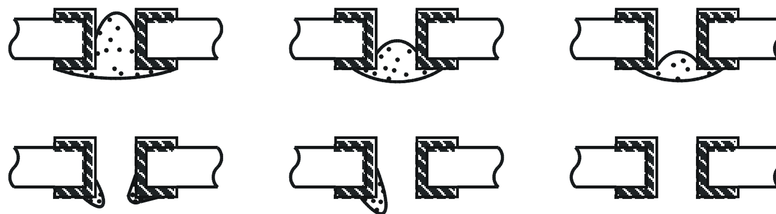


Acceptable Holes
Showing that the coated or applied solder has wetted sides of holes and tops of lands



Not Acceptable Holes
Showing that the applied solder has not wetted sides of holes

00102601

Figure 1 Effectiveness of Solder Wetting of Plated-through Holes

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